REMARKS

Reconsideration and allowance are respectfully requested in view of the following remarks.

Claims 1-19 were rejected under 35 U.S.C. 102(b) as being anticipated by Tassan Caser. Applicants respectfully traverse.

Turning first to claim 1, Applicants have amended claim 1 to clarify the nature and relationship between the first and second regulation stages.

More specifically, Applicants claim that the first regulation stage generates an output voltage for the programming phase of non volatile memory cells. The circuits in Tassan Caser which generate the programming phase voltage are the pump 15, upper regulator 23 and switch program 68. The pump 15 and upper regulator 23 together generate a regulated high voltage hv. The switch program 68 component receives that voltage hv and functions through enable circuit 44 along with the slope resistance 46 and capacitance C_L to generate the programming phase signal voltage (see, Table 1, Vp, col. 6, lines 56-63) as shown in Figure 6.

Applicants further claim that the second regulation stage generates an output voltage for the soft programming phase of non volatile memory cells. The circuit in Tassan Caser which generate the soft programming phase voltage is the lower regulator 27. The lower regulator 27 also receives the voltage hv, but it functions to generate the soft programming voltages (see, Table 1, Vsp, col. 9, lines 42-47).

With foregoing in mind, Applicants still further claim "the generated output voltage from the first stage being a supply voltage for said second stage." This limitation is neither disclosed

nor suggested by Tassan Caser. Rather, it is quite clear from Figure 7 that the lower regulator 27 receives the high voltage hv as its supply voltage (see, also, Figure 8). Claim 1, on the contrary, recites that it is the generated first regulation stage output voltage which is the second regulation stage supply voltage. In Tassan Caser, the generated first regulation stage output voltage is Vxreg (see, Figure 5). It clear, however, from a review of Figures 3 and 7 that Vxreg is not the supply voltage for the lower regulator 27 (i.e., the second regulation stage).

In this regard, the Examiner is invited to compare the power supply teachings of Tassan Caser with respect to the voltage hv to Applicants' specification and in particular node 3 of Figure 5 in the application. Figure 5 illustrates that which is recited in claim 1; namely, that the generated first regulation stage output voltage (at node 3, from stage ST1) is the power supply voltage for the second regulation stage (see, source terminals of the transistors in the current mirror 2). No such circuit is disclosed or suggested by Tassan Caser.

Applicants accordingly respectfully submit that claim 1 is not anticipated by Tassan Caser.

Turning next to claim 2, Applicants further claim that the "second stage comprises a current mirror structure." Again, the second regulation stage in Tassan Caser is the lower regulator 27 which functions to generate the soft programming voltages (see, Table 1, Vsp, col. 9, lines 42-47). A review of Figure 7 of Tassan Caser fails to reveal the presence of a current mirror. Applicants accordingly submit that claim 2 is not anticipated by Tassan Caser. A similar argument is made in favor of new claim 20.

In view of the foregoing, Applicants respectfully submit that claims 1-6 are patentable over Tassan Caser.

Turning next to claim 7, Applicants claim "a first voltage regulation stage that generates a voltage ramp output at a first output." The Examiner points to the pump 15 and upper regulator 23. The circuit 15/23 of Tassan Caser functions to generate a stable 12V high reference voltage hv. There is no teaching or suggestion in Tassan Caser for the high voltage hv being "a voltage ramp." Rather, it is clear that the voltage ramp is instead generated by the switch program 68 component which receives that voltage hv and functions through enable circuit 44 along with the slope resistance 46 and capacitance C_L to generate the programming phase signal voltage (see, Table 1, Vp, col. 6, lines 56-63) as shown in Figure 6. Thus, only the circuits 15/23/68 together can meet the claimed "first voltage regulation stage" limitation.

Applicants further claim "a second voltage regulation stage that generates a regulated voltage output at a second output" This limitation could be met by the lower regulator 27 of Tassan Caser.

With foregoing in mind, Applicants still further claim "a selection switch that responds to a control signal to selectively connect the first output to the second output." The first output of the circuits 15/23/68 is node 67, while the second output of circuit 27 is node 36. A review of Figure 3 in Tassan Caser fails to reveal any switch or other circuitry which selectively connects nodes 67 and 36 to each other. Rather, Tassan Caser appears to teach shorting those nodes together (see, also, col. 4, lines 65-67). This is quite different from the claimed invention.

In this regard, the Examiner is invited to compare the output circuit teachings of Tassan Caser with respect to nodes 67 and 36 to Applicants' specification and in particular node 3 and node 13 of Figure 5 in the application. Figure 5 illustrates that which is recited in claim 7; namely, the presence of a "selection switch" in the form of transistor 4 gate controlled by a control signal "Softp." No such output selection circuit is disclosed or suggested by Tassan Caser.

Applicants accordingly respectfully submit that claim 7 is not anticipated by Tassan Caser.

Turning next to dependent claim 11, Applicants further claim that "the first output of the first voltage regulation stage is a power supply for the second voltage regulation stage." As discussed in detail above in connection with claim 1, there is no teaching or suggestion in Tassan Caser for this limitation. Rather, it is quite clear that the first and second voltage regulation stages in Tassan Caser each receive the regulated high voltage hv at their respective power supplies. The output at node 67 from circuit 68 in Tassan Caser is not a power supply for the circuit 27.

With respect to claim 12, Applicants submit that this claim is patentable over the art for at least the same reasons as claim 2 in that there is no teaching or suggestion, given correct identification of the first and second regulators, for the claimed second voltage regulation stage comprising a current mirror circuit.

In view of the foregoing, Applicants respectfully submit that claims 7-12 are patentable over the Tassan Caser.

Turning next to claims 13-15, Applicants submit that this claim is patentable over Tassan Caser for at least the same reasons as claim 7 in that there is no teaching or suggestion, given correct identification of the first and second regulators, for the claimed "selection circuit."

With respect to claim 16 and 20, Applicants submit that this claim is patentable over Tassan Caser for at least the same reasons as claims 1 and 11 in that there is no teaching or suggestion, given correct identification of the first and second regulators, for the claimed limitation of "wherein the first output of the first regulator is a power supply for the second regulator."

In view of the above, it is believed that this application is in condition for allowance, and such a Notice is respectfully requested.

Respectfully submitted,

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Date: 3/3/06

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